# GaNSlim™ HFQR/CCM Control

## 1. Features

### GaNSlim™ Power FET

- Loss-less current sensing
- Low Rdson power FET
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating

### High Frequency QR/CCM Controller

- Wide VDD range up to 77.5V
- QR valley switching and CCM operating modes
- High frequency operation
- High voltage start-up
- Optimized driver and frequency hopping for low EMI
- OVP, UVP, OTP, LPS protection functions
- Ultra-low standby current consumption

### DPAK-4L Package with Grounded Cooling Pad

- Minimized package inductance
- Low thermal resistance

### High Power Density

- High power density
- Small transformer size
- Low component count

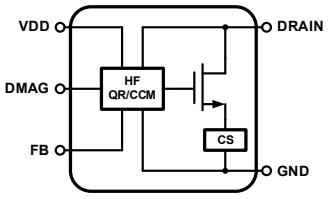
### Product Reliability

- 20-year limited product warranty (see Section 14 for details)

## 2. Topologies / Applications

- High efficiency AC-DC power adapters
- USB PD/QC battery charger
- Auxiliary power for servers, white goods.


DPAK-4L

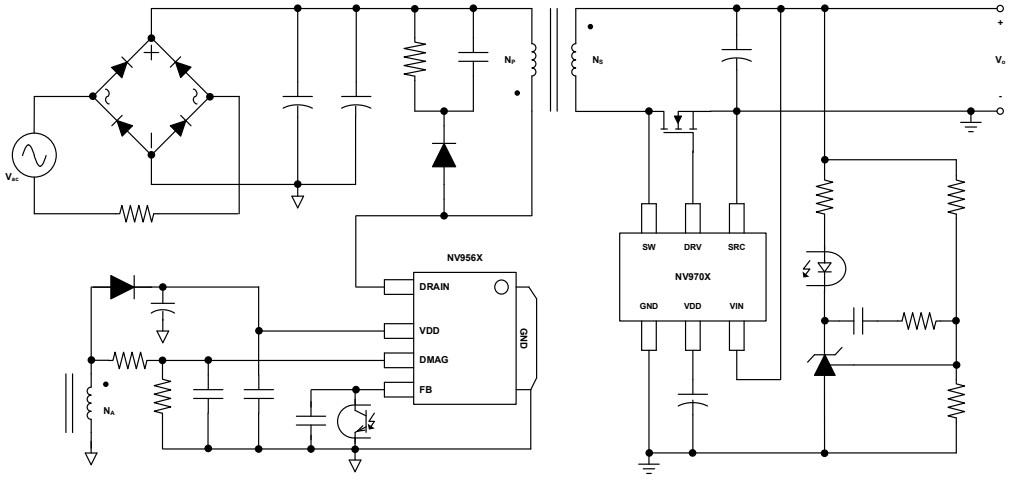



Simplified schematic

## 3. Description

This GaNSlim™ HFQR/CCM controller integrates a high performance eMode GaNSlim Power FET together with an HFQR/CCM Flyback controller to achieve unprecedented high-frequency and high-efficiency operation for smallest size mobile charger and adapter solutions. The GaNSlim Power FET includes loss-less current sensing, ultra-low gate charge, low output charge, and 700V continuous and 800V transient voltage ratings to provide excellent performance and robustness. The HFQR/CCM Flyback controller enables high frequency operation, wide VDD range, high-voltage start-up, and multi-mode operation. The HFQR/CCM Flyback controller also includes abnormal component short-circuit, over-temperature and LPS protection features to increase system robustness, while ultra-low standby current consumption increases light, tiny & no-load efficiency. Low-profile, low-inductance, and DAPK-4L packaging enables designers to achieve simple, quick and reliable solutions. Navitas' GaN IC technology enables high frequencies, high efficiencies, and low EMI to achieve unprecedented power densities at a very attractive cost structure.

## 4. Typical Application Circuit




Flyback Application Schematic

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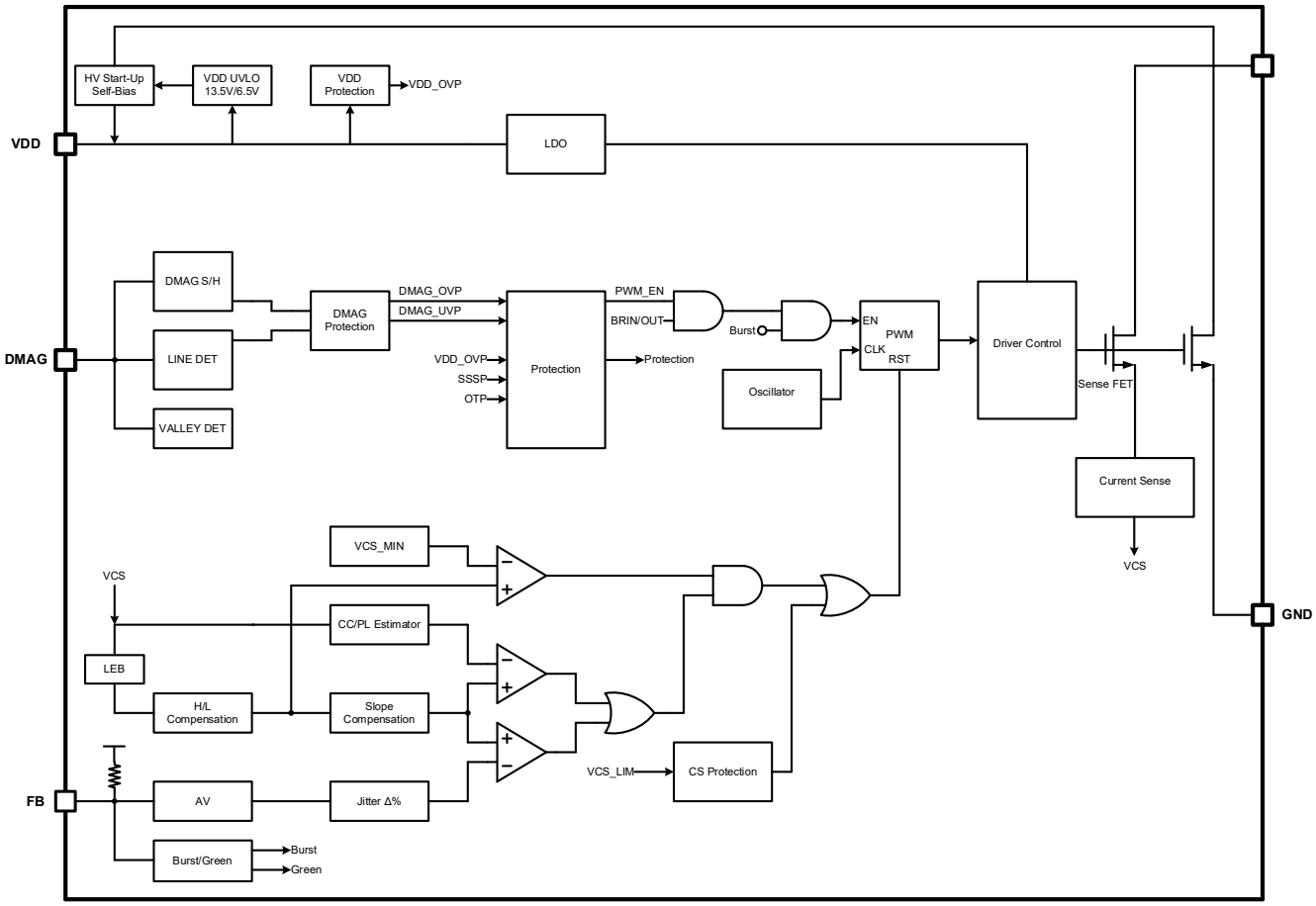
## 6. Ordering Information

| Part Number | Maximum Frequency | $R_{DS(ON)}$ | Typ. Internal Rcs (Ω) | Typ. Primary Current Limit Ip (A) | Mode & Protection | Operating Temperature Range | Package | Packing Method Tape &Reel |
|---|---|---|---|---|---|---|---|---|
| NV9563L05C | 125kHz | 330mΩ | 1050 | 2.79 | QR LAR | -40°C to +125°C | DAPK-4L | 2,000: 13” Reel |
| NV9563C00C | 125kHz | | 1000 | 2.93 | CCM+QR LAR | | | |

LAR: Long Auto-Restart Mode

## 7. Internal Functional Block Diagram



# 8. Specifications

## 8.1. Absolute Maximum Ratings (1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DS(CONT)}$ | GaN Power FET Continuous Drain-to-Source Voltage (2) | | -7 | 700 | V |
| $V_{DS(TRAN)}$ | GaN Power FET Transient Drain-to-Source Voltage (3) | | - | 800 | V |
| $V_{VDD}$ | VDD DC Supply Voltage | | -0.3 | 80 | V |
| $V_{FB}$ | FB Pin Input Voltage | | -0.3 | 5.5 | V |
| $V_{DMAG}$ | DMAG Pin Input Voltage | | -0.3 | 5.5 | V |
| $I_D$ | GaN Power FET Continuous Drain Current. (@$T_C$ = 100ºC) | | - | 4 | A |
| $I_D$ PULSE | GaN Power FET Pulsed Drain Current (10 µs @ $T_J$ = 125ºC) | | - | 8 | A |
| $T_J$ | Operating Junction Temperature | | -40 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -40 | 150 | °C |
| $T_L$ | Lead Temperature (Soldering) 10 Seconds | | - | 260 | °C |
| ESD | Electrostatic Discharge Capability | Human Body Mode, ANSI/ESDA/JEDEC JS-001-2024 | | 1.5 | kV |
| | | Charge Device Mode, ANSI/ESDA/JEDEC JS-002-2025 | - | 1.0 | kV |

*Note (1): Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device*

*Note (2): $V_{DS(CONT)}$ rating is specified for GaN Power FET*

*Note (3): $V_{DS(TRAN)}$ rating is specified for GaN Power FET and allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption) and repetitive events that are <400ns (for example repetitive leakage inductance spikes).*

## 8.2. Recommended Operating Conditions (4)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Navitas does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{VDD}$ | VDD Pin Supply Voltage | -0.3 | | 75 | V |
| $V_{FB}$ | FB Pin Supply Voltage | -0.3 | | 5 | V |
| $V_{DMAG}$ | DMAG Pin Supply Voltage | -0.3 | | 5 | V |

*Note (4): Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +125°C unless otherwise noted.*

## 8.3. Thermal Resistance (5)

| Symbol | Parameter | Typ. | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Case | 9.64 | ºC/W |
| $R_{\theta JC}$ | Junction-to-Ambient | 52.96 | ºC/W |

*Note (5) $R_{\theta}$ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)*

## 8.4. Electrical Specifications

$V_{DD}$ (Typ.) = 12V, and $T_A$ (Typ.) = 25°C, unless otherwise specified.

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **HV Section** | | | | | | |
| $I_{HV}$ | Supply Current Drawn from Drain Pin | $V_{DRAIN}$=50 V, $V_{DD}$=0 V | 2 | 5 | 10 | mA |
| $I_{HV-LC}$ | Leakage Current Drawn from Drain Pin | $V_{DRAIN}$=50 V, $V_{DD}$=$V_{DD\_UVLO}$+1 V | | | 3 | μA |
| **VDD Section** | | | | | | |
| $V_{DD\_ON}$ | $V_{DD}$ Turn-On Threshold Voltage | $V_{DD}$ Rising | 12.0 | 13.5 | 15.0 | V |
| $V_{DD\_UVLO}$ | $V_{DD}$ UVLO Threshold Voltage | | 6.3 | 6.5 | 6.8 | V |
| $I_{DD\_ST}$ | Startup Current | | 0.5 | 2 | 5 | μA |
| $I_{DD\_OP}$ | Operating Supply Current | No DRV Switching | 0.60 | 0.75 | 0.85 | mA |
| $I_{DD\_DPGN}$ | Operating Supply Current in Deep Green-Mode | | 200 | 300 | 400 | μA |
| $V_{DD\_OVP}$ (6) | $V_{DD}$ Over-Voltage-Protection Threshold | | 77 | 78.5 | 80 | V |
| $t_{D\_UVLO}$ (6) | UVLO De-bounce Time | | | 10 | | μs |
| $t_{D\_VDD\_OVP}$ (6) | $V_{DD}$ Over-Voltage-Protection De-bounce Time | | | 15 | | μs |
| $t_{VDD\_LAR}$ | Long Auto-Restart Mode Time | Trim Option | 1.38 | 1.64 | 1.90 | s |
| **Oscillator Section** | | | | | | |
| $f_{S\_TMO}$ | Minimum Time-Out Frequency | | 24 | 25 | 26 | kHz |
| $f_{S\_CRM}$ | Minimum CRM Frequency | | 14.2 | 15.6 | 17 | kHz |
| $f_{S\_BNK\_MAX}$ | Maximum Blanking Frequency | Option:125kHz | 115 | 125 | 135 | kHz |
| | | Option:175kHz | 160 | 175 | 190 | kHz |
| | | Option:225kHz | 205 | 225 | 245 | kHz |
| $f_{S\_CCM\_MAX}$ | Maximum CCM Frequency | Option:125kHz | 95.9 | 104 | 112.5 | kHz |
| | | Option:175kHz | 133.4 | 145.8 | 158.2 | kHz |
| $t_{ON\_MAX}$ | Maximum PWM ON Time Opt1 | Option:125kHz | 16.2 | 17.6 | 19 | μs |
| | | Option:175kHz, 225kHz | 8.6 | 9.6 | 10.6 | μs |
| $D_{MAX}$ | Maximum Duty Cycle in CCM | While CCM is disabled, no $D_{MAX}$ $V_{OSC-DMAX}$=0.625V | 71 | 75 | 79 | % |
| $\Delta V_{JIT}$ | Current Sense of Jitter Range | Low line<br>High line | | +/-3.85<br>+/-7.7 | | % |
| $t_{JIT}$ | Frequency Jitter Period | | 0.5 | 0.60 | 0.7 | ms |
| $\Delta f_{JIT\_CCM}$ | CCM Jitter Range | | | +/-3.85 | | % |

## Electrical Specifications (cont.)

$V_{DD}$ (Typ.) = 12V, and $T_A$ (Typ.) = 25°C, unless otherwise specified.

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Feedback Section** | | | | | | |
| $V_{FB\_OPEN}$ | FB Open Voltage | | 5.00 | 5.20 | 5.40 | V |
| $Z_{FB}$ | FB Pull Up Resistor | | 36 | 40 | 48 | kΩ |
| $A_V$ (6) | FB Voltage Attenuation Factor | | 0.185 | 0.200 | 0.215 | V/V |
| $V_{FB\_GRN\_ENT}$ | FB Threshold for Green Mode Entry | | 1.550 | 1.600 | 1.650 | V |
| $V_{FB\_GRN\_EXT}$ | FB Threshold for Green Mode Exit | | 1.650 | 1.700 | 1.750 | V |
| $V_{FB\_BST\_ENT}$ | FB Threshold for Burst Mode Entry | | 0.650 | 0.700 | 0.750 | V |
| $V_{FB\_BST\_EXT}$ | FB Threshold for Burst Mode Exit | | 0.700 | 0.750 | 0.800 | V |
| $V_{FB\_BNK\_STR}$ | Frequency Foldback Start Point | | 2.225 | 2.300 | 2.375 | V |
| $V_{FB\_BNK\_END\_125kHz}$ | Frequency Foldback End Point | Option:125kHz, 175kHz | 1.475 | 1.550 | 1.625 | V |
| $V_{FB\_BNK\_END\_225kHz}$ | Frequency Foldback End Point | Option:225kHz | 1.425 | 1.500 | 1.575 | V |
| $t_{D\_DPGN}$ | Debounce Time to Enter Deep Green Mode | | 120 | 160 | 200 | µs |
| $V_{FB\_OLP}$ | FB Threshold for OLP Exit | | 3.5 | 3.6 | 3.7 | V |
| | FB Threshold for OLP Enter | | 3.8 | 3.9 | 4.0 | V |
| $t_{D\_OLP}$ | OLP Protection De-bounce Time | | 32 | 36 | 40 | ms |
| **Over-Temperature Protection Section** | | | | | | |
| $T_{OTP}$ | Over-Temperature-Protection Threshold | | 125 | 140 | 155 | °C |
| $\Delta T_{OTP}$ (6) | Over-Temperature-Protection Hysteresis | | | 20 | | °C |

## Electrical Specifications (cont.)

$V_{DD}$ (Typ.) = 12V, and $T_A$ (Typ.) = 25°C, unless otherwise specified.

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DMAG Section** | | | | | | |
| $I_{DMAG\_Max}$ | Maximum Guaranteed Operating Current Flow Out of DMAG Pin | | 1.94 | | | mA |
| $I_{DMAG\_BRI}$ | Current Threshold for Brown-In | | 0.432 | 0.480 | 0.528 | mA |
| $N_{BRI}$ | Debounce Cycle for Brown-In | | | 4 | | Cycle |
| $I_{DMAG\_BRO}$ | Current Threshold for Brown-Out | | 0.396 | 0.440 | 0.484 | mA |
| $t_{D-BRO}$ | Debounce Cycle for Brown-Out | | 15 | 16.5 | 18 | ms |
| $I_{DMAG\_HL}$ | Current Threshold for High Line ($164V_{AC}$) | | 1.008 | 1.120 | 1.232 | mA |
| $N_{HL\_ENT}$ | Debounce Cycle for High Line Entry | | | 4 | | Cycle |
| $I_{DMAG\_LL}$ | Current Threshold for Low Line ($153V_{AC}$) | | 0.936 | 1.04 | 1.144 | mA |
| $t_{D-LL\_ENT}$ | Debounce Cycle for Low Line Entry | | 15 | 16.5 | 18 | ms |
| $V_{DMAG\_HV}$ | $V_{DMAG}$ Threshold for High Output | | 1.65 | 1.75 | 1.85 | V |
| $V_{DMAG\_LV}$ | $V_{DMAG}$ Threshold for Low Output | | 1.50 | 1.60 | 1.70 | V |
| $V_{DMAG\_LV\_HYS}$ | $V_{DMAG}$ Hysteresis Threshold for Low Output | | | 0.150 | | V |
| $N_{DMAG\_HV\_LV}$ | Debounce Cycle for High/Low Output Change | | | 4 | | Cycle |
| $V_{DMAG-UVP}$ | $V_{DMAG}$ Under-Voltage-Protection Threshold | | 0.390 | 0.425 | 0.460 | V |
| $N_{DMAG\_UVP}$ | Debounce Cycle for $V_{DMAG\_UVP}$ | | | 2 | | Cycle |
| $t_{VDMAG\_UVP\_BNK}$ | $V_{DMAG\_UVP}$ Blanking Time during Start-up | | 27.5 | 32 | 36.5 | ms |
| $V_{DMAG\_OVP}$ | $V_{DMAG}$ Over-Voltage-Protection Threshold | | 3.45 | 3.55 | 3.65 | V |
| $N_{DMAG\_OVP}$ | Debounce Cycle for $V_{DMAG\_OVP}$ | | | 2 | | Cycle |
| $t_{DMAG\_BNK\_L}$ | DAMG Sampling Blanking Time $V_{FB}<V_{FB\_GRN\_ENT}$(1.60V) | Option:125kHz | | 0.96 | | µs |
| | | Option:175kHz,225kHz | | 0.48 | | µs |
| $t_{DMAG\_BNK\_M}$ | DAMG Sampling Blanking Time $V_{FB}>V_{FB\_GRN\_EXT}$ (1.70V) | Option:125kHz | | 1.6 | | µs |
| | | Option: 175kHz,225kHz | | 1.07 | | µs |

## Electrical Specifications (cont.)

$V_{DD}$ (Typ.) = 12V, and $T_A$ (Typ.) = 25°C, unless otherwise specified.

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Current Sense Section** | | | | | | |
| $Gain_{CS}$ | Current Sense Ratio $I_{CS}/I_{DRAIN}$ | | | 4500 | | A/A |
| $R_{EFF}$ | Effective Sense Resistor | | | $R_{CS}$/Gaincs | | Ω |
| Ip | Primary Current Limit | Rcs=1050 | 2.53 | 2.79 | 3.04 | A |
| | | Rcs=1000 | 2.66 | 2.93 | 3.19 | A |
| $I_{BST}$ | Primary Current at Burst Mode | | | 0.385*Ip | | A |
| $t_{LEB}$ | Leading Edge Blanking Time | | | 265 | | ns |
| $t_{PD}$ | Propagation Delay from CS to DRV | | | 65 | | ns |
| **GaN Power FET Section** | | | | | | |
| Typical conditions: $V_{DS}$ = 400V, $F_{SW}$ = 1MHz, $T_{AMB}$ = 25°C, unless otherwise specified | | | | | | |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$ = 650V, FET OFF | | 0.15 | 25 | μA |
| $R_{DS(ON)}$ | Drain-Source Resistance | | | 330 | 462 | mΩ |
| $V_{SD}$ | Source-Drain Reverse Voltage | | | 3.5 | | V |
| $Q_{OSS}$ | Output Charge | $V_{DS}$ = 400 V, FET OFF | | 7.2 | | nC |
| $Q_{RR}$ | Reverse Recovery Charge | | | 0 | | nC |
| $C_{OSS}$ | Output Capacitance | $V_{DS}$ = 400 V, FET OFF | | 9.7 | | pF |
| $C_{O\ (er)}$ (7) | Effective Output Capacitance, Energy Related | $V_{DS}$ = 400 V, FET OFF | | 13 | | pF |
| $C_{O\ (tr)}$ (7) | Effective Output Capacitance, Time Related | $V_{DS}$ = 400 V, FET OFF | | 18 | | pF |

*Note (6): Guaranteed by design*

*Note (7): $C_{O\ (er)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

*$C_{O\ (tr)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

## 8.5. Characteristic Graphs

($T_C$ = -40 to 125 ºC unless otherwise specified)

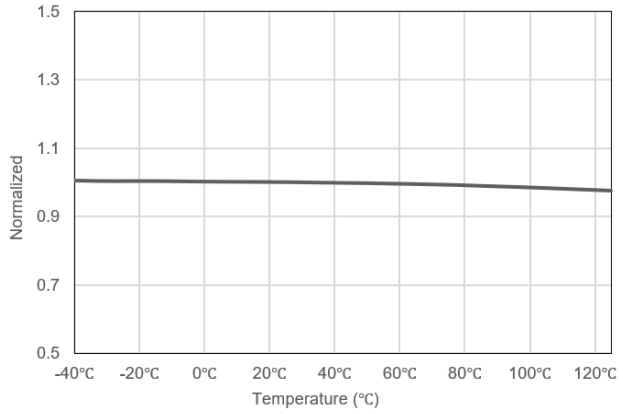



Fig. 1. $V_{DD\_ON}$

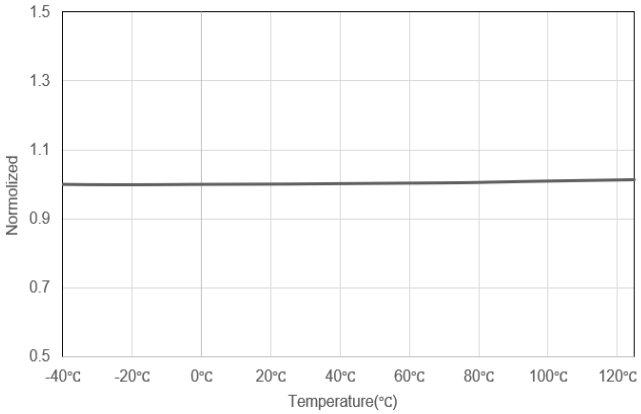



Fig. 2. $V_{DD\_UVLO}$

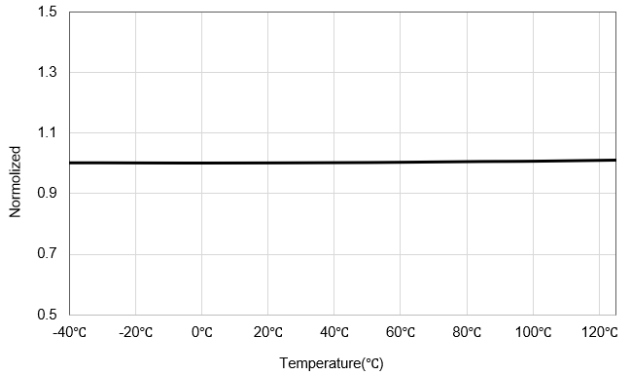



Fig. 3. $V_{DD\_OVP}$

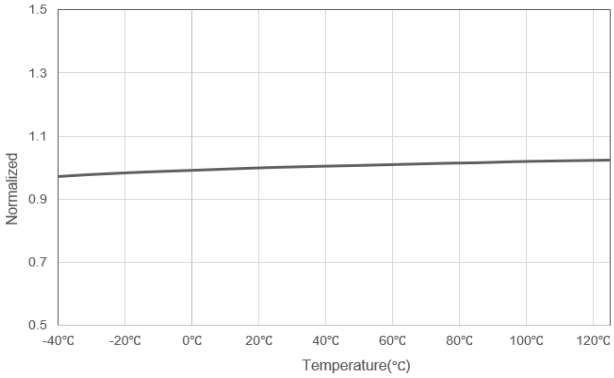



Fig. 4. $f_{S\_TMO}$

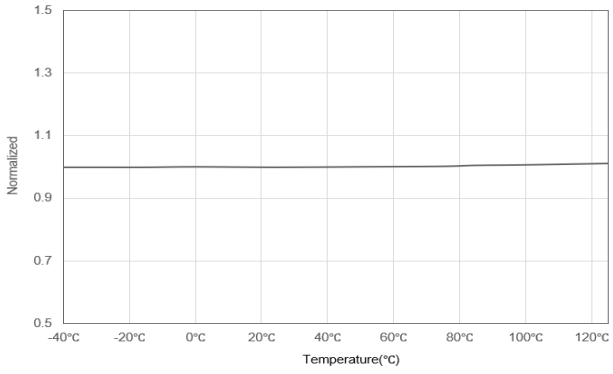



Fig. 5. $V_{FB\_BST\_ENT}$

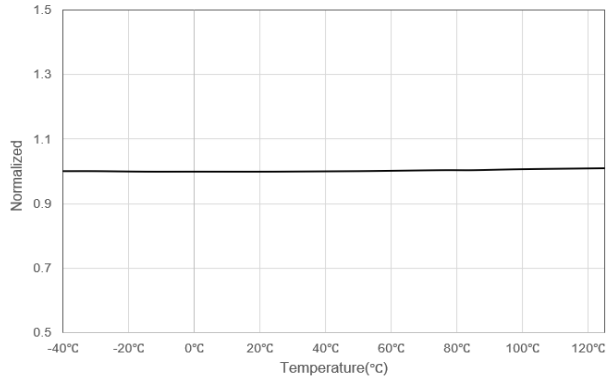



Fig. 6. $V_{FB\_BST\_EXT}$

## Characteristic Graphs (cont.)

($T_C$ = -40 to 125 ºC unless otherwise specified)

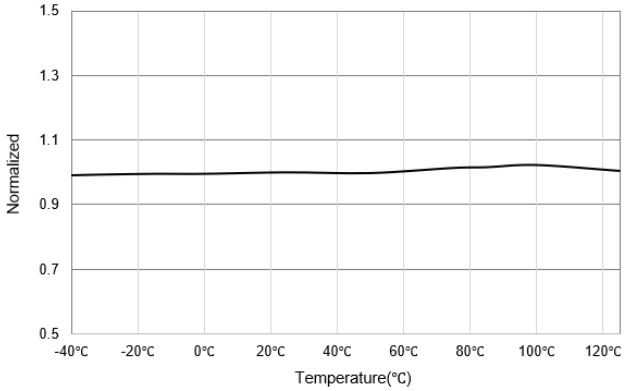



Fig. 7. $I_{DMAG\_BRI}$

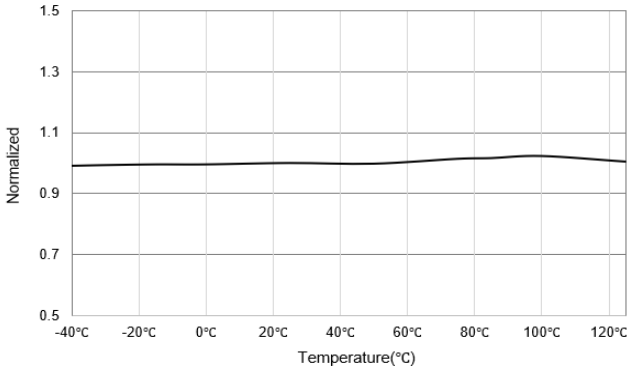



Fig. 8. $I_{DMAG\_BRO}$

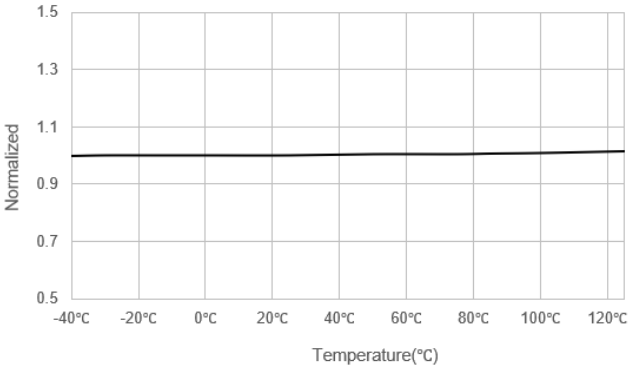



Fig. 9. $V_{DMAG\_UVP}$

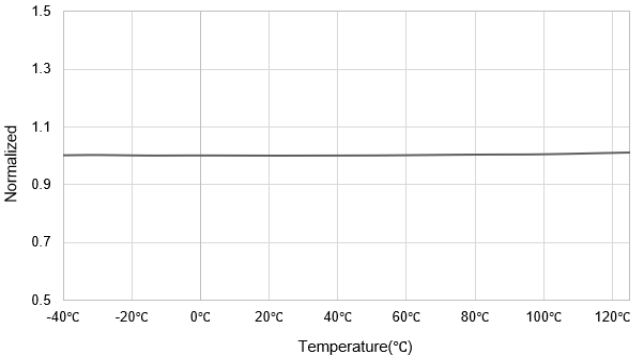



Fig. 10. $V_{DMAG\_OVP}$

## Characteristic Graphs (Cont.)

($T_C$ = 25 ºC unless otherwise specified)

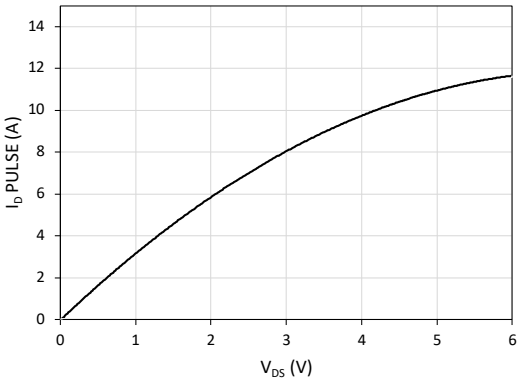



Figure 11. Pulsed Drain current ($I_D$ PULSE) vs. drain-to-source voltage ($V_{DS}$) at T =25 °C

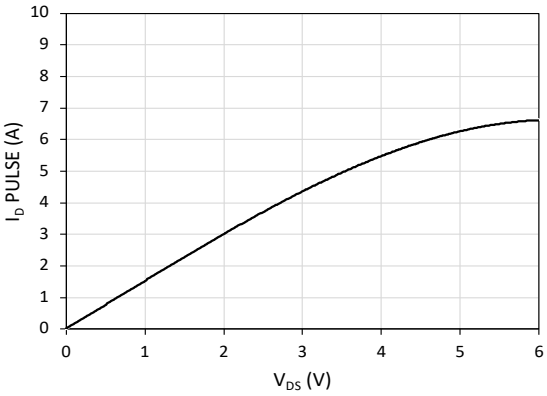



Figure.12. Pulsed Drain current ($I_D$ PULSE) vs. drain-to-source voltage ($V_{DS}$) at T =125 °C

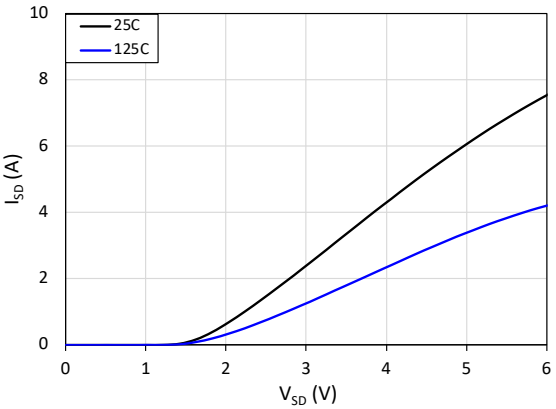



Figure 13. Source-to-drain reverse conduction voltage

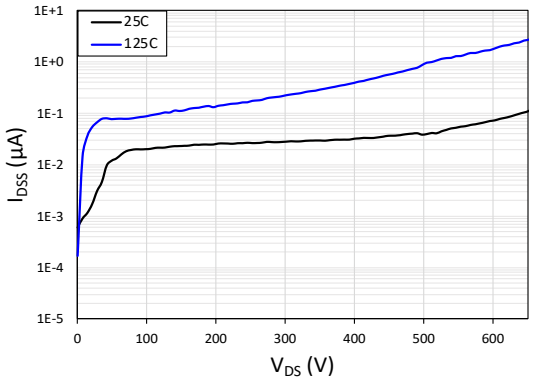



Figure 14. Drain-to-source leakage current ($I_{DSS}$) vs. drain-to-source voltage ($V_{DS}$)

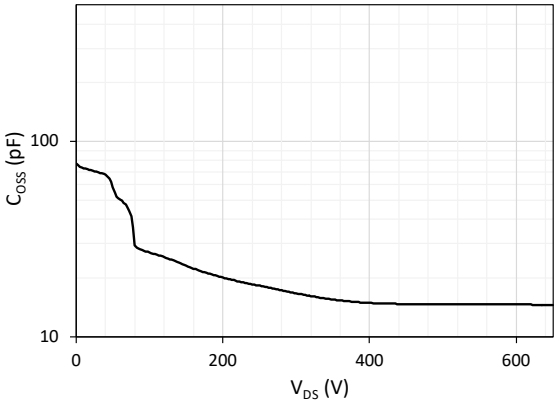



Figure 15. Output capacitance ($C_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)

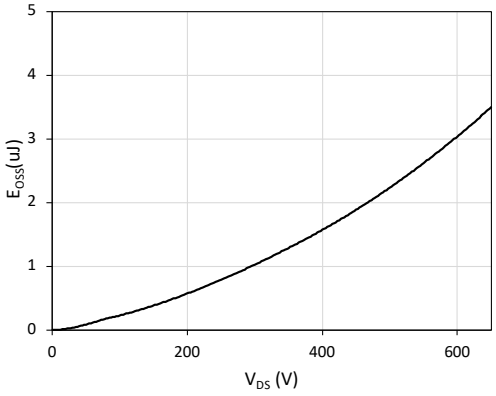



Figure 16. Energy stored in output capacitance ($E_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)

## Characteristic Graphs (Cont.)

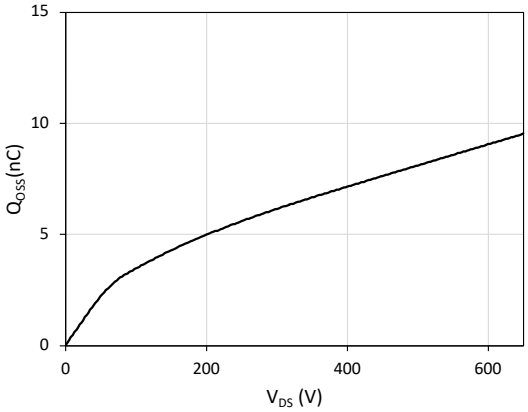



Figure 17. Charge stored in output capacitance ($Q_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)

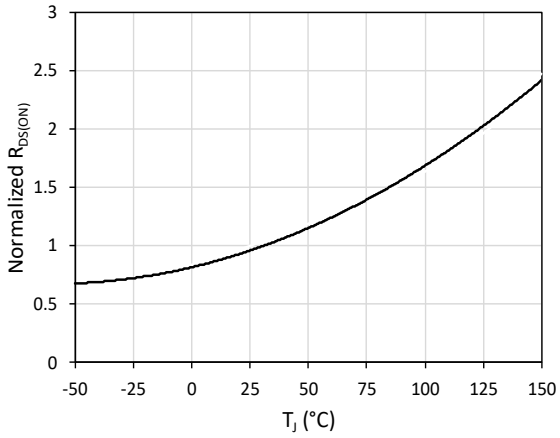



Figure 18. Normalized on-resistance ($R_{DS(ON)}$) vs. Junction temperature ($T_J$)

## 9. Pin Configurations and Functions

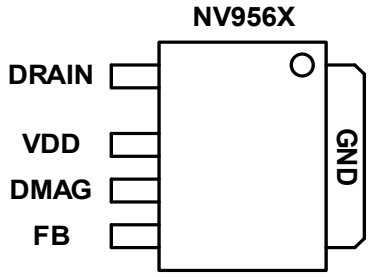



Fig. 19. Pin Configuration (Top View)

| Pin No. | Name | Description |
|---|---|---|
| 1 | DRAIN | **Drain of GaN Power FET.** This pin is also connected internally to the high-voltage startup circuit. |
| 2 | VDD | **Power Supply**. IC operation current and GaN FET driving current are supplied through this pin. Typically, this pin is connected to an external $V_{DD}$ capacitor. The device starts to operate when $V_{DD}$ exceeds 13.5V. |
| 3 | DMAG | **Demagnetization Sense**. This pin is used to detect resonant valleys for QR switching. It also detects the output voltage information, as well as the input voltage information for Brown-in & Brown-out protection. |
| 4 | FB | **Feedback**. Input for the internal PWM comparator. |
| Body | GND | **Ground.** Source of Power FET and IC supply ground. Metal pad on bottom of package. |

## 10. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality.

### Basic Operation

NV956x family ICs are offline flyback regulators which operate in frequency limit quasi-resonant (QR) mode to reduce switching losses and EMI (electromagnetic interference). It regulates the output based on the load condition through feedback circuitry.

The QR resonant frequency is determined by the transformer primary inductance ($L_p$) and the primary side GaN FET effective output capacitance ($C_{oss\text{-}eff}$).

$$C_{oss-eff} = C_{oss-GaNFET} + C_{parasitic} + C_{transformer} \quad \text{(Equation 1)}$$

$$t_{resonance} = 2\pi\sqrt{L_p \times C_{oss-eff}} \quad \text{(Equation 2)}$$

In a general 956x design at no load or light load condition, the frequency limit $f_{S\_BNK}$ for the pulse-to-pulse operating frequency is $f_{S\_TMO}$ So operating frequency is between $f_{S\_TMO}$ and 1/ ($1/f_{S\_TMO}$ + $t_{resonance.}$). At the medium load condition (e.g.25%~50% of full load), the frequency limit $f_{S\_BNK}$ is modulated as a function of load condition such that it varies between $f_{S\_TMO}$ and $f_{S\_BNK\_MAX\_LL(HL)}$ as load varies. At the heavy load condition (e.g. 50%~100% of full load), $f_{S\_BNK}$ is fixed at $f_{S\_BNK\_MAX\_LL(HL)}$ such that the switching frequency is not higher than $f_{S\_BNK\_MAX}$ as shown in the figure below.

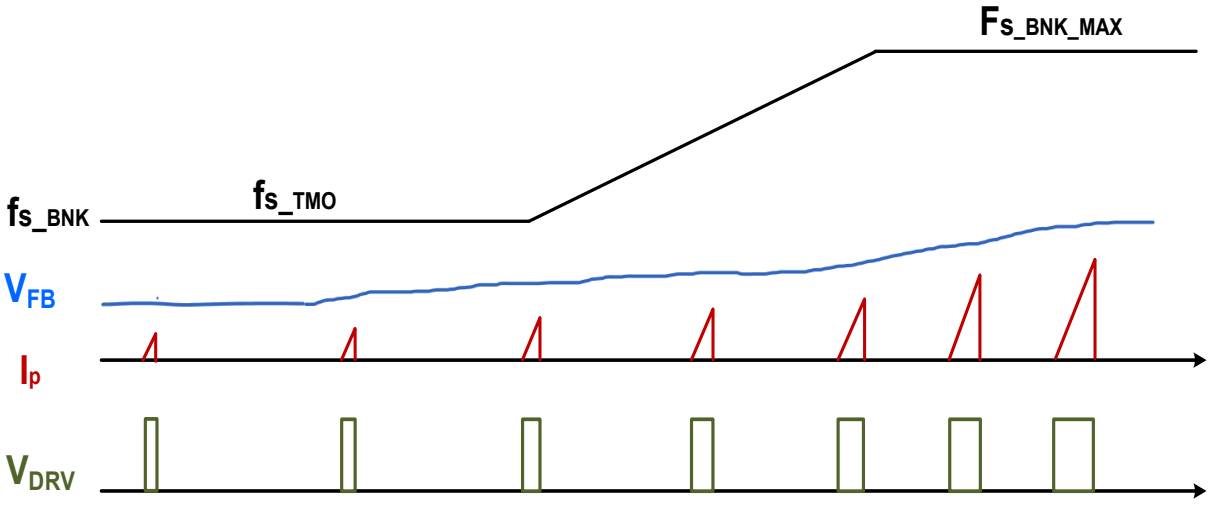



**Figure 20 Frequency Fold-Back Operation**

NV956x family ICs also have option to operate in CCM at low line. When the device enters CCM, the maximum CCM frequency limit is $f_{S\_BNK\_MAX\_CCM}$.

### Burst Mode

As shown in Figure 21, when feedback voltage $V_{FB}$ drops below $V_{FB\_BST\_ENT}$ at light load, the PWM output shuts off and the output voltage drops at a rate depending on current level of the load. Thereafter, the voltage of feedback-$V_{FB}$ rises. Once $V_{FB}$ exceeds $V_{FB\_BST\_EXT}$, NV956x family products resume switching and the switch peak currents is limited by $V_{CS\_MIN}$. If more power is delivered to the load than required, $V_{FB}$ voltage will decrease. Once $V_{FB}$ voltage is pulled below $V_{FB\_BST\_ENT}$, switching stops again. In this manner, the burst mode operation alternately enables and disables switching of the GaN FET to regulate the output and in the meanwhile reduce the switching losses.

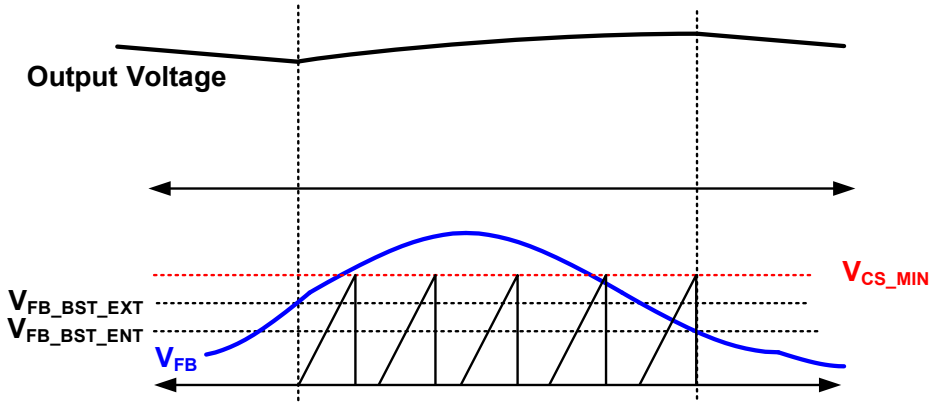



**Figure 21 Burst Mode Operation**

### Deep Green Mode

NV956x family ICs enter the deep green mode if $V_{FB}$ voltage stays below $V_{FB\_BST\_ENT}$ for more than $t_{D\_DPGN}$. In the deep green mode, the IC operating current is reduced to $I_{DD\_DPGN}$ to minimize power consumption. IC resumes switching with normal operating current $I_{DD\_OP}$ once $V_{FB}$ voltage rises above $V_{FB\_BST\_EXT}$.

### Valley Detection

NV956x family valley detection is achieved by monitoring $V_{DMAG}$ voltage, which is the divided auxiliary winding voltage by $R_{DMAG1}$ and $R_{DMAG2}$ as shown in figure below. One ceramic capacitor ($C_{DMAG}$) with typical value of 10pF (and not bigger than 22pF) is recommended to filter out the noise if there is PCB noise coupling concern.

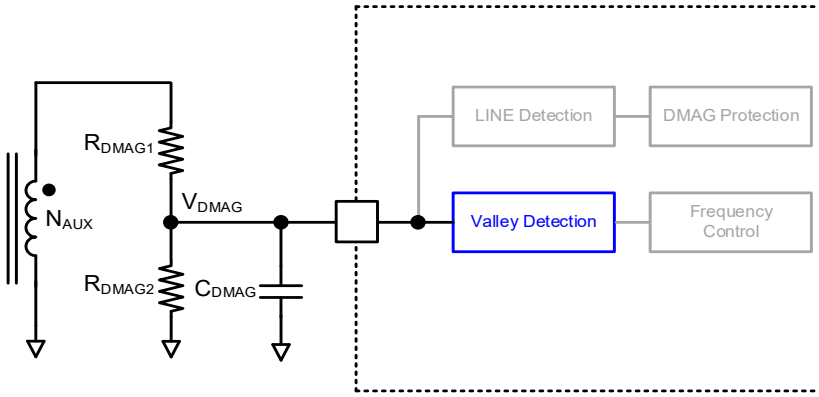



**Figure 22 Valley Detection Circuit**

### Frequency Jitter

To help system to meet stringent EMI requirements, NV956x features advanced frequency jittering to average the energy peaks over the EMI frequency range.

### Output Voltage Detection

NV956x family products detect output voltage through DMAG voltage. The figure below shows the DMAG voltage ($V_{DMAG-S/H}$) sampled at the end of $t_{DMAG\_BNK}$ to avoid sampling errors. The DMAG voltage is set based on the transformer turn ratio, the voltage divider resistors $R_{DMAG1}$ & $R_{DMAG2}$. The ratio ($Ratio_{DMAG}$) between $V_{DMAG-S/H}$ and Vo can be defined as:

$$Ratio_{DMAG} = \frac{V_{DMAG-S/H}}{V_O} = \frac{N_A}{N_S} \times \frac{R_{DMAG2}}{R_{DMAG1} + R_{DMAG2}} \quad \text{(Equation 3)}$$

$Ratio_{DMAG}$ is required to be designed to guarantee Vo nominal operation will not hit protection, i.e., $V_{DMAG-S/H}$ will not hit either $V_{DMAG-OVP}$ or $V_{DMAG-UVP}$ described in protection section. For USB-PD/PPS applications, a typical recommended $Ratio_{DMAG}$ design is 0.16.

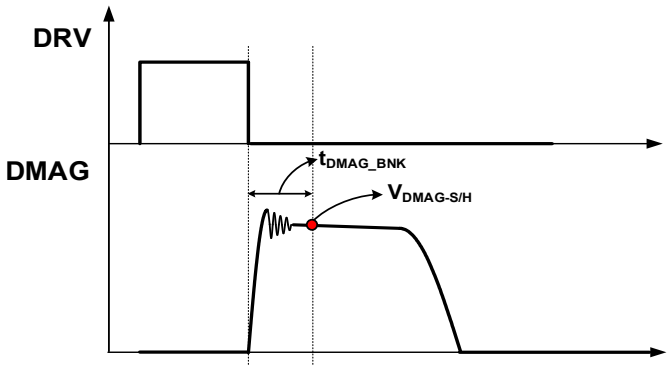



**Figure 23 Output Voltage Detection**

### Line Voltage Detection

As illustrated in Figure 24, NV956X family products indirectly sense the line voltage through DMAG pin during GaN FET turn-on period. During the GaN FET conduction time, the line voltage detector clamps DMAG pin voltage at 0V. The auxiliary winding voltage, $V_{AUX}$, is proportional to the input bulk capacitor voltage, $V_{BLK}$. So current $I_{DMAG}$ flowing out of DMAG pin is expressed as:

$$I_{DMAG} = \frac{V_{BLK}}{R_{DMAG1}} \times \frac{N_A}{N_P} \quad \text{(Equation 4)}$$

$I_{DMAG}$ current, reflecting the line voltage information, is used for the brown-in and brown-out protection.

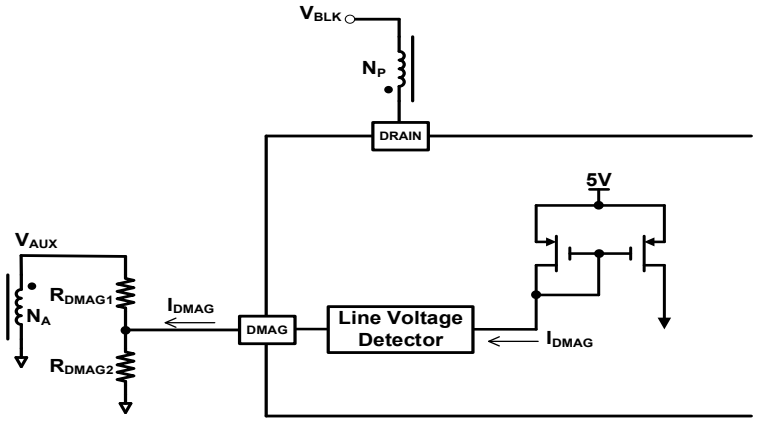



**Figure 24 Line Voltage Detection Circuit**

### LPS Function

NV956X family products incorporate built-in circuits to limit output power and limit output current in the event of the protocol IC becoming malfunction.

### HV Start-up

During startup, the internal HV startup circuit is enabled, and the input voltage supplies the current, $I_{HV}$, from drain pin to charge hold-up capacitor $C_{VDD}$. When $V_{DD}$ voltage reaches $V_{DD\_ON}$, the HV startup circuit is disabled. The IC starts PWM switching and senses DMAG signal to check the brown-in condition. If the brown-in is not detected, the IC enters the auto-restart mode. The HV startup circuit is connected to the Drain pin

### Protection Description

NV956X family products protection functions include VDD over-voltage protection (VDD-OVP), Brown-out protection, DMAG over-voltage protection (DMAG-OVP), DMAG under-voltage protection (DMAG-UVP), IC internal over-temperature protection (OTP). All protections have auto-restart and long auto-restart mode. The selected option information is provided on page 3.

When the long auto-restart mode protection is triggered, the integrated GaN FET is turned off for a time period of $t_{VDD\_LAR}$). After $t_{VDD\_LAR}$, if VDD rises above $V_{DD\_ON}$, NV956X family products resume normal operation as shown in the figure below.

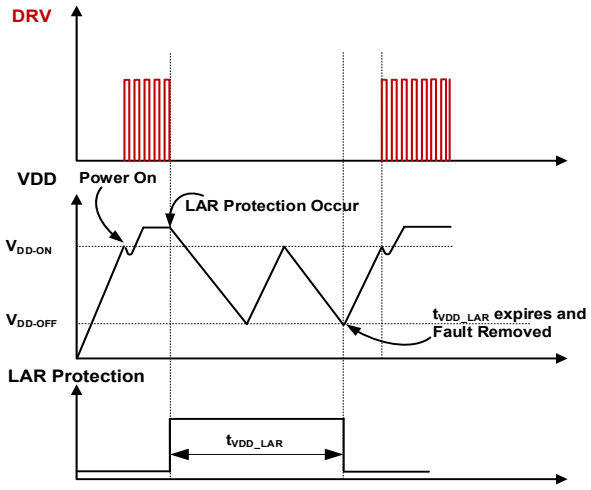



**Figure 25 Auto-Restart Long AR Mode**

### VDD-OVP

VDD-OVP prevents IC damage from over voltage stress when abnormal system conditions occur. When VDD voltage exceeds $V_{DD\_OVP}$ for the debounce time $t_{D\_VDD\_OVP}$, the VDD-OVP protection is triggered, the device enters protection mode.

### Brown-in & Brown-out

The sensed line voltage information is used for the brown-in and brown-out protection. During GaN FET conduction time, when the current $I_{DMAG}$ flowing out of DMAG pin is higher than $I_{DMAG\_BRI}$ for $N_{BRI}$ debounce cycles, the brown-in is enabled. The input bulk capacitor voltage level to enable the brown-in is given as

$$V_{BLK\_Brownin} = I_{DMAG\_BRI} \times \frac{R_{DMAG1}}{N_A/N_P} \quad \text{(Equation 5)}$$

When $I_{DMAG}$ is lower than $I_{DMAG\_BRO}$ for longer than $t_{D\_BRO}$, the brown-out is triggered. The input bulk capacitor voltage level to trigger the brown-out protection is given as

$$V_{BLK\_Brownout} = I_{DMAG\_BRO} \times \frac{R_{DMAG1}}{N_A/N_P} \quad \text{(Equation 6)}$$

### IC Internal OTP

The internal temperature-sensing circuit disables the PWM output if the junction temperature exceeds $T_{OTP}$, and the IC enters protection mode.

### DMAG-OVP

DMAG-OVP prevents server system damage when abnormal system conditions occur and cause DMAG voltage to rise abnormally. Usually, DMAG over voltage protection is caused by not working properly feedback network (FB) or a fault condition of the DMAG voltage divider resistors. Figure below shows the internal circuit of DMAG-OVP. When abnormal system conditions occur and cause DMAG voltage to exceed $V_{DMAG\_OVP}$ for more than $N_{DMAG\_OVP}$ consecutive switching cycles, PWM pulses are disabled, and the IC enters protection mode.

For DMAG voltage divider design, $R_{DMAG1}$ is obtained from Equation 5, and $R_{DMAG2}$ is determined by Equation 3. The output over voltage protection level, $V_{O\_OVP}$, can be determined by Equation 7.

$$V_{O\_OVP} = \frac{N_S}{N_A} \times (1 + \frac{R_{DMAG1}}{R_{DMAG2}}) \times V_{DMAG\_OVP} \quad \text{(Equation 7)}$$

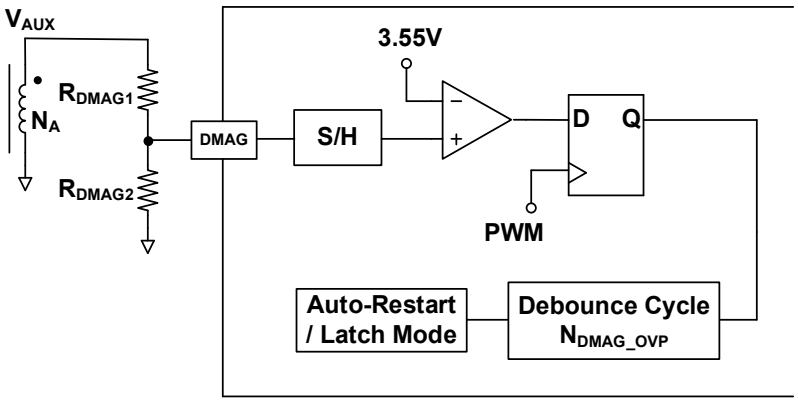



**Figure 26 DMAG Over Voltage Protection Circuit**

**DMAG-UVP**

In the event with short output, the output voltage will drop, and the primary peak current will increase. To prevent operation for a long time under this condition, NV956x family products incorporate the under-voltage protection through DMAG pin (DMAG-UVP). The figure below shows the internal circuit for DMAG-UVP. When DMAG voltage is less than $V_{DMAG\_UVP}$ and longer than de-bounce cycles $N_{DMAG\_UVP}$, DMAG UVP is triggered, and the IC enters protection mode.

The output under voltage protection level, $V_{O\_UVP}$, can be determined by Equation 8.

$$V_{O\_UVP} = \frac{V_{DMAG_{UVP}}}{Ratio_{DMAG}} = \frac{N_S}{N_A} \times (1 + \frac{R_{DMAG1}}{R_{DMAG2}}) \times V_{DMAG\_UVP} \quad \text{(Equation 8)}$$

To avoid DMAG-UVP triggering during the startup sequence, startup blanking time $t_{VDMAG\_UVP\_BNK}$ is incorporated for system power on.

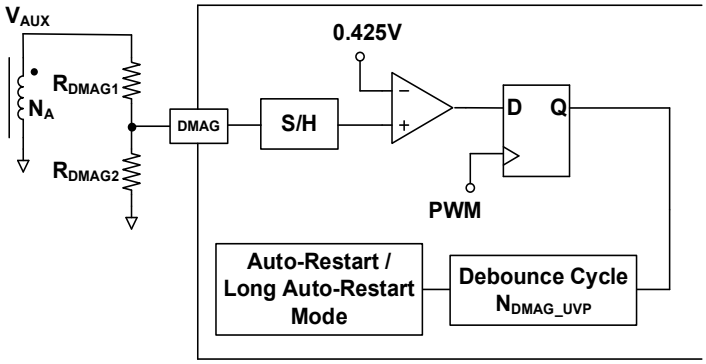



**Figure 27 DMAG Under Voltage Protection Circuit**

**Cycle by Cycle Current Limit**

Under certain operation conditions, such as the startup or the overload condition, the feedback control loop can be saturated and is unable to control the primary peak current. To limit the current under such conditions, NV956X family products incorporate the cycle-by-cycle current protection which forces the GaN switch turn off when power FET current reaches the current limit Ip.

**GaN Power FET Drain-to-Source Voltage Considerations**

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 33. When the device is switched off, the energy stored in the transformer leakage inductance will cause $V_{DS}$ to overshoot to the level of $V_{SPIKE}$. The clamp circuit should be designed to control the magnitude of $V_{SPIKE}$. After dissipation of the leakage energy, the device $V_{DS}$ will settle to the level of the bus voltage plus the reflected output voltage which is defined in the figure below as $V_{DS-OFF}$.

- For repetitive events, 80% derating should be applied from $V_{DS\ (TRAN)}$ rating (800V) to 640V max under the worst-case operating conditions.
- It is recommended to design the system such that $V_{DS-OFF}$ is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge-based topologies, such as LLC, $V_{DS}$ voltage is clamped to the bus voltage. $V_{DS}$ should be designed such that it meets the $V_{DS-OFF}$ derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive $V_{SPIKE}$ durations < 100 µs. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes).

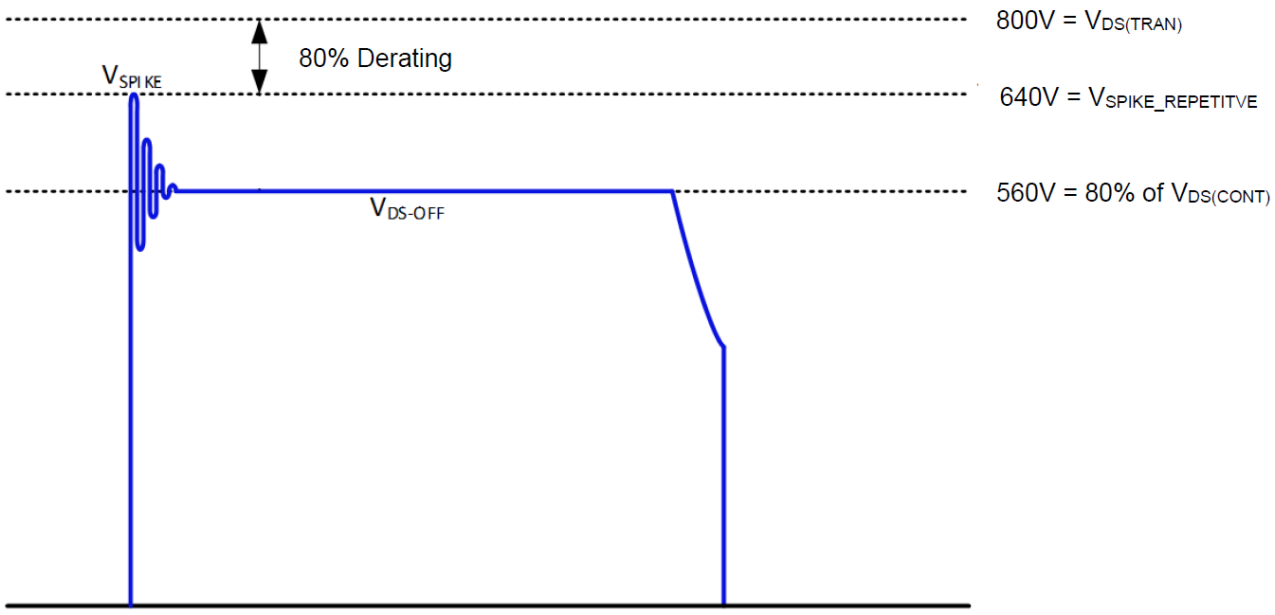
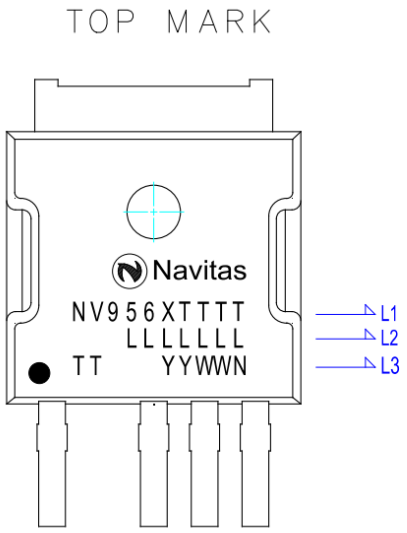


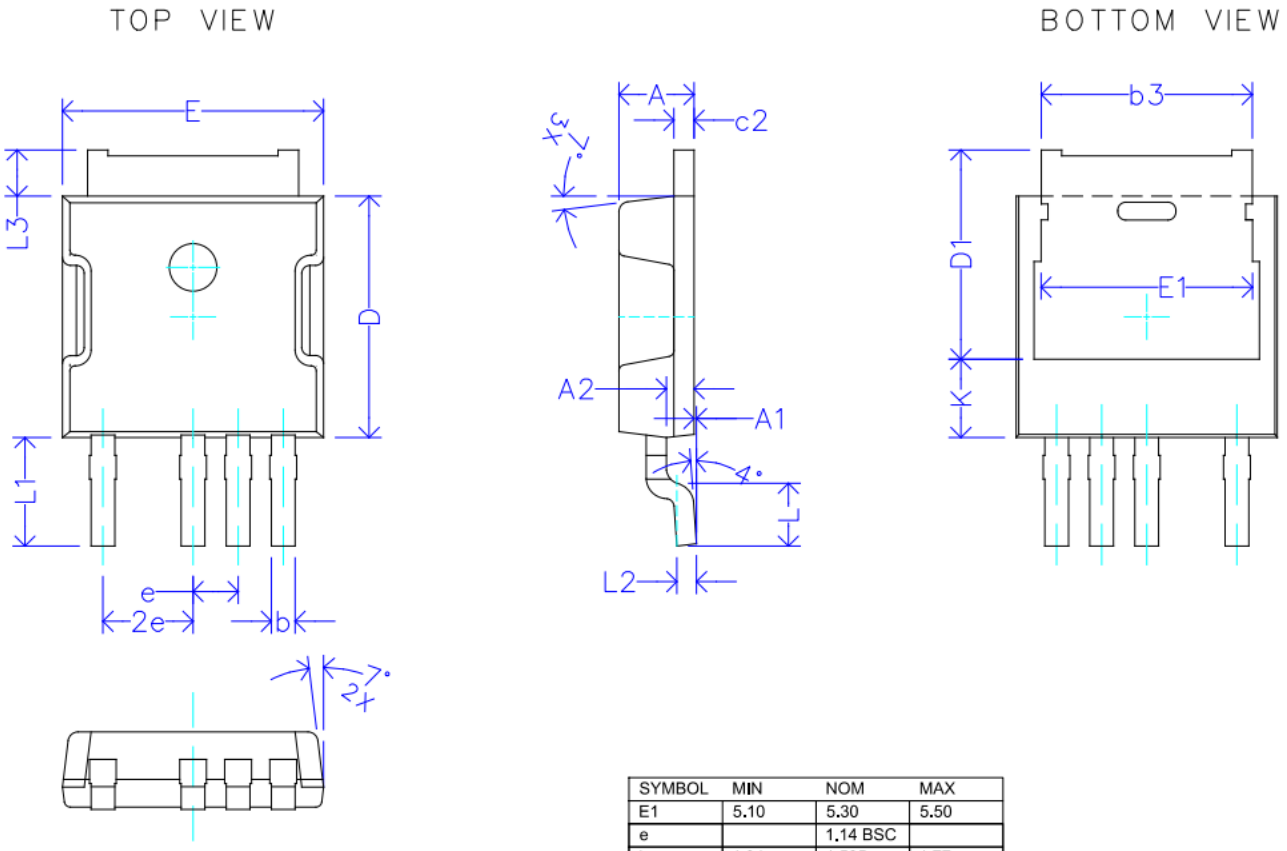

**Figure 28 QR flyback drain-to-source voltage stress diagram**

## 11. Package Outline (DPAK-4L)




| Marking Line | Marking Symbol | Content Description |
|---|---|---|
| L1 | NV956XTTTT | Part Number : First 10 digits of part number, where TTTT trim code of device. (If device name is 12 digits, last 2 digits for special parts will be printed in the 3rd line TT where is bank for general parts) |
| L2 | LLLLLLL | Lot Number : Max 7 digits assembly lot number for marking<br>Example : NC31900 |
| L3 | TT | Optional Trim Code : Last 2 digits of device name incase device name is 12 digits |
| | YY | Year Code : Last 2 digits of the year<br>Example : 2023, YY=23 |
| | WW | Week Code : 01 - 53 |
| | N | Supplier Site Code : Y = HYME |

## 11. Package Outline (Cont.)

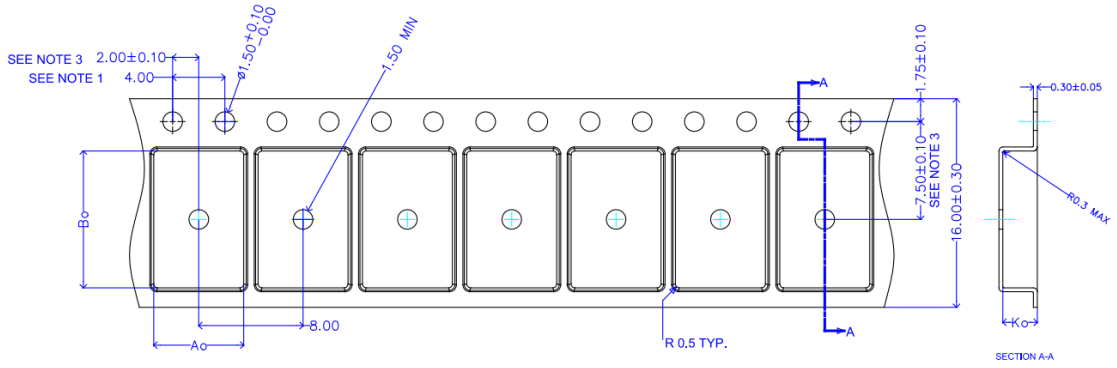



| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.80 | 1.90 | 2.00 |
| A1 | 0.00 | - | 0.20 |
| A2 | 0.60 | 0.70 | 0.80 |
| b | 0.508 | 0.60 | 0.711 |
| b3 | 5.21 | - | 5.46 |
| c2 | 0.41 | 0.508 | 0.61 |
| D | 6.00 | 6.10 | 6.22 |
| D1 | 4.90 | - | - |
| E | 6.40 | 6.60 | 6.73 |

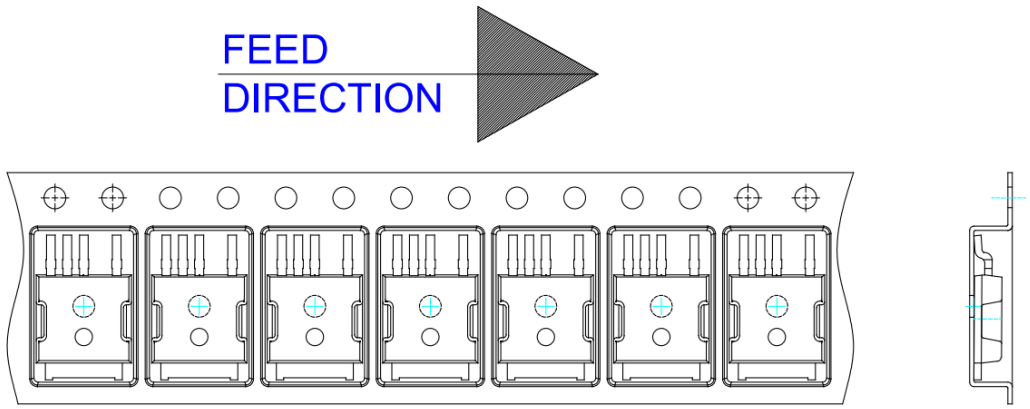
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| E1 | 5.10 | 5.30 | 5.50 |
| e | | 1.14 BSC | |
| L | 1.34 | 1.585 | 1.77 |
| L1 | | 2.743 REF | |
| L2 | 0.41 | 0.508 | 0.61 |
| L3 | 0.88 | - | 1.28 |
| K | 1.98 | - | - |
| Package Draft Angles | | 5-9 degrees | |
| Foot Angle | | 0-8 degrees | |
| Gauge Plane for L | | 0.508 | |

Notes :
1. All dimentions in mm.
2. Reference JEDEC TO-252F VAR AD
3. 100% Sn Plating

## 12. Tape and Reel Dimensions



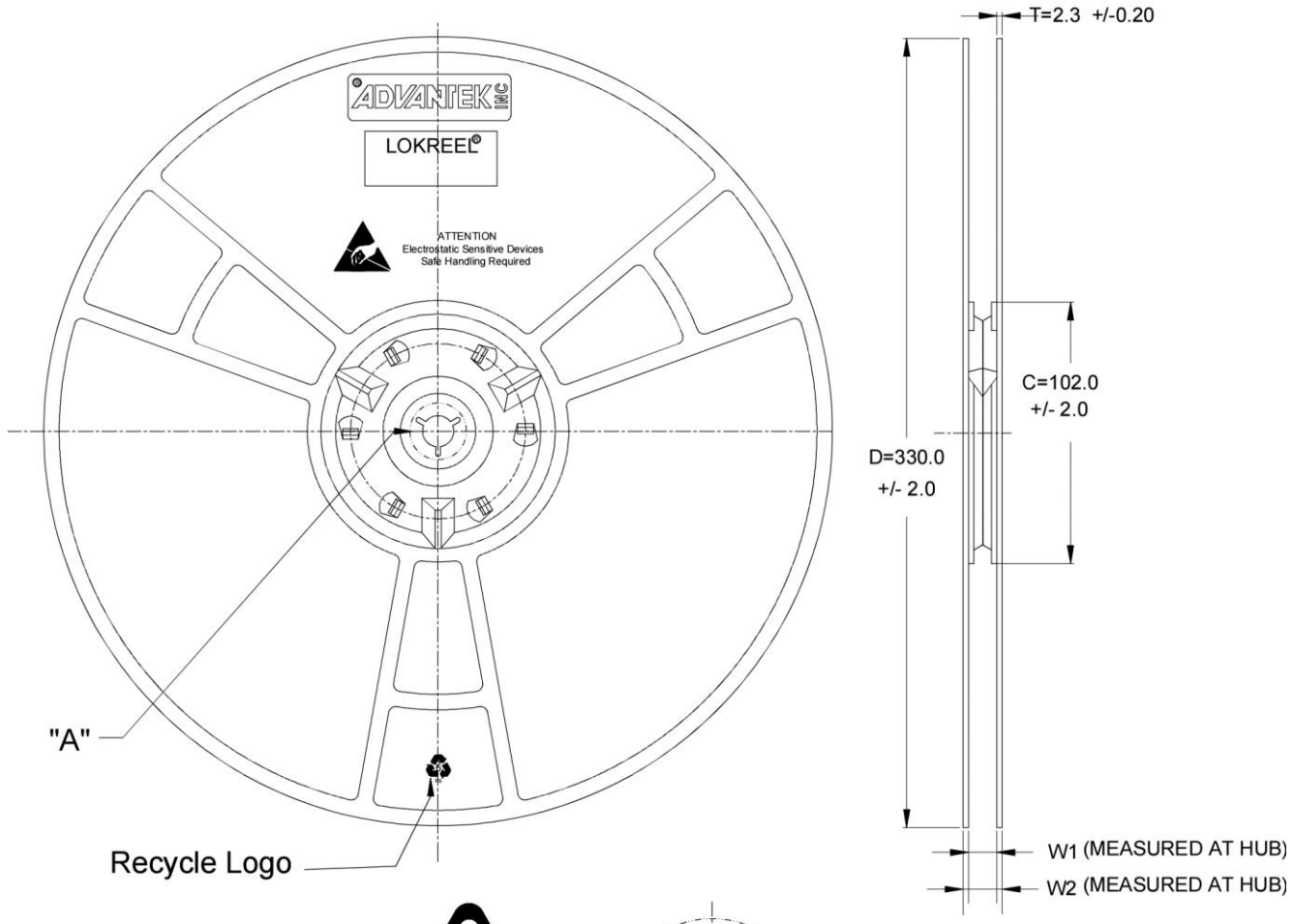

| Notes | |
|---|---|
| Ao | 6.9 |
| Bo | 10.50 |
| Ko | 2.65 |
| 1. 10 sproket hole pitch cumulative tolerance ±0.2 | |
| 2. Camber in compliance with EIA 481 | |
| 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole. | |




| Reel Quantity | | Pin 1 Orientation |
|---|---|---|
| Reel Size | Unit qty in reel | 2 1 / 3 4 Pin 1 on quadrant 1 |
| 13 " | 2500 units | |
| Leader and trailer pocket : 50 empty pockets | | |

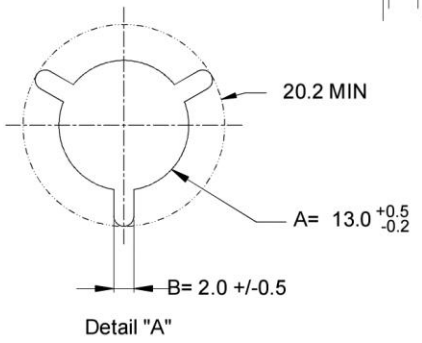
## 12. Tape and Reel Dimensions (Cont.)

-All Dimensions in Millimeters-





Recycle Logo




Detail "A"

Note:
1. RB: Regrind Blue Lokreel
2. RBK: Regrind Black Lokreel
3. RC: Conductive Lokreel
4. SW: White Lokreel
5. SW-BL: Blue Lokreel

5.1 Suffix "DBK" : Black Reel ; 1x 10 Exp 5 ≤ SR < 1 x 10 Exp 10 ohms/sq.

6. RD Series Lokreel: 1x 10 Exp 5 ≤ SR<1 x 10 Exp 12 ohms/sq.
7. RC Series Lokreel: SR< 1 x 10 Exp 5 ohms/sq.

| Nominal Hub Width | W1 | W2 MAX |
|---|---|---|
| 12mm | 12.8mm +1.6 / -0.4 | 18.4mm |

## 13. 20-Year Limited Product Warranty

The 20-year limited warranty applies to all packaged Navitas GaNFast Power ICs and GaNSense HFQR Controllers in mass production, subject to the terms and conditions of, Navitas' express limited product warranty, available at https://navitassemi.com/terms-conditions. The warranted specifications include only the MIN and MAX values only listed in Absolute Maximum Ratings and Electrical Characteristics sections of this datasheet. Typical (TYP) values or other specifications are not warranted.


## 14. Revision History

| Date | Status | Notes |
|---|---|---|
| 10-11-2025 | Datasheet | First publication |
| | | |
| | | |
| | | |
| | | |
| | | |

## Additional Information



Contact info@navitassemi.com